International Journal of Electronics and Communication Engineering (IJECE)
ISSN 2278-9901
Vol. 2, Issue 4, Sep 2013, 75-84

International Academy of Science, Engineering and Technology
Connecting Researchers; Nurturing Innovations

AUTONOMOUS MODULATION DETECTION WITH S3C2440 PROCESSOR AND OPEN SOURCE MODULES

R. KANNAN[1] & S. RAVI[2]

[1]Research Scholar, Department of ECE, Sathyabama University, Chennai, Tamil Nadu, India

[2]Professor and Head, Department of ECE, M.G.R University, Chennai, Tamil Nadu, India

ABSTRACT

The digital world, with or without the use of interconnected networks is influenced by channel conditions and maintaining the required throughput and quality of service is challenging. In this paper, automatic detection of modulation techniques with hardware implementation is presented. The modulated techniques used for the classification is binary phase shift keying, binary amplitude phase shift keying, pulse width modulation, quadrature amplitude modulation and frequency shift keying. The hardware is implemented on S3C2440 (FL2440) processor. The performance evaluation of the proposed system is carried using various test signals. Experimental results show that the proposed method is able to perform autonomous detection.

KEYWORDS: Automatic Modulation Detection, FL2440 Hardware, GNU Radio

INTRODUCTION

Software defined radio (SDR) is an important element of wireless technology with rapid strides in the telecommunication field. Determining the digital hardware composition of a software radio is a key design step in its creation.SDR provides an efficient and protected solution to the problem of building multi-mode, multi-band and multifunctional wireless communication devices.

Design and implementation of wireless Turbo Code OFDM (TC-OFDM) on the small form factor Software defined Radio (SDR) Platform, provided by Lyrtech and Texas Instrument is presented in [1]. TC-OFDM is proposed in dissimilar channels communication system in order to decrease the bit error rate. The performance analysis is evaluated by simulations in different channels including AWGN and multipath Rayleigh fading channel. By the evaluation TC-OFDM gives the better performance than single carrier OFDM system in multipath Rayleigh fading channels. On the other hand, Turbo codes can eliminate the residual inter symbol interference (ISI) and inter channel interference (ICI) and therefore reduce the length of the required cyclic prefix in an OFDM system.

A practical design and implementation procedure for a wireless digital modem on software defined radio platforms and reports a detailed description is presented in [2] of the baseband signal processing logic design in the FPGA portion of it. Design verification is performed through hardware in the loop testing methodology. A framework for designing wireless digital modems on hybrid software radio platforms is discussed. The design and FPGA implementation of discrete wavelet transforms (DWT) for real-time infrasound data processing is presented in [3].This approach uses only two FIR filters, a high-pass and a low-pass filter. A compact execution was realized with pipelining techniques and multiple uses of generalized building blocks. The design was described in VHDL and the FPGA implementation and simulation were performed on the QUARTUS II platform.

A modulation level classifier based on the abridged complexity Kuiper test is implemented in [4]. The BEE2

hardware prototyping platform and its performance are evaluated. In particular, the classification accuracy of the proposed classifier in distinctive among 4, 16, and 64-QAM is analyzed under varying SNR, varying number of symbols, and different timing offsets. The performance of the proposed classifier is compared to that of the widely-used Cumulant-based classifier. Possible architectures are proposed, and their classification accuracy and computational complexity are compared. The two classifiers have comparable hardware utilizations.

Support Vector Machines are emerging as a powerful machine learning tool. Logarithmic Number Systems (LNS) utilize the property of logarithmic compression for numerical operations. An implementation of a digital Support Vector Machine (SVM) classifier using LNS in which considerable hardware savings are achieved with no significant loss in classification accuracy is discussed in [5].

A novel algorithm for multiple signal classification with optimized coulomb energy neural networks for power line communications is presented in [6]. The algorithm entails structured preprocessing of the received signals, and ensemble them further for effective classification using a novel Optimized Coulomb Energy Neural Network (OCENN). The simulation and experimental results obtained shows an accuracy of more than 97% which is much better than the results of the comparative hardware approaches, which are costly and difficult to implement. It has been noticed that noise and attenuation experienced over the power line affecting the higher frequency signals does not have an impact on our classification procedure, thus providing a robust architecture for implementation of PLC.

A powerful and flexible digital signal processing (DSP) architecture based on the Texas Instruments TMS320VC33 DSP and high speed PCI bus is presented in [7]. The DSP board provides a convenient, flexible means to test signal processing algorithms in real-time hardware. Algorithms implemented for several research projects include normalized least mean square (NLMS) adaptive filter, recurrent neural network (RNN), Viterbi decoding, and adaptive beam forming.

A real-time digital signal processor (DSP)-based hierarchical neural network classifier capable of classifying both analog and digital modulation signals is discussed in [8]. A high-performance DSP processor, namely the TMS320C6701, is utilized to implement different kinds of classifiers including a hierarchical neural network classifier. A total of 31 statistical signal features are extracted and used to classify 11 modulation signals plus white noise.

A coherent neural net based framework for solving various signal processing problems. It relies on the assertion that time-lagged recurrent networks possess the necessary representational capabilities to act as universal approximators of nonlinear dynamical systems are explained in [9]. This applies to system identification, time-series prediction, nonlinear filtering, adaptive filtering, and temporal pattern classification.

A software radio and a software radio technique for automatic digital modulation scheme recognition is presented in [10]. The modulation recognition technique is designed for a real-time software radio using general-purpose processors and is based on a modified pattern recognition and phase classifier approach. One test scenario, where an intercepted signal is either BPSK or QPSK modulated, using an AWGN channel with random phase noise shows that correct modulation scheme classification is possible to a lower-bound channel SNR of approximately 9dB.

INTELLIGENT RECEIVER WITH AUTOMATIC MODULATION RECOGNITION

The automatic recognition of the modulation format of a detected signal, the intermediate step between signal detection and demodulation, is a major task of an intelligent receiver. Obviously, with no knowledge of the transmitted data and many unknown parameters at the receiver, such as the signal power, carrier frequency and phase offsets, timing

information, etc., blind identification of the modulation is a difficult task. This becomes even more challenging in real-world scenarios with multipath fading, frequency-selective and time-varying channels. In general, AMC is a challenging task, especially in a non-cooperative environment, where in addition to multipath propagation, frequency-selectivity and time-varying nature of the channel, no prior knowledge of the incoming signal is available. A classifier is supposed to correctly choose the modulation format of the incoming signal from a pool of N mod candidate modulations. The focus is on algorithms for ASK, PSK, QAM, and FSK classification we have considered the most intuitive way to identify the modulation class of the incoming signal is to use the information contained in its instantaneous amplitude, phase and frequency. FSK signals are characterized by constant instantaneous amplitude, whereas ASK signals have amplitude fluctuations, and PSK signals have information in the phase. The maximum of the discrete Fourier transform (DFT) of centered (average or first order moment) normalized instantaneous amplitude was used as a feature to distinguish between FSK and ASK/ PSK classes.

The Automatic modulation detection extracts about seven parameters (Features based on amplitude, frequency and phase) for identification of different modulation techniques stated as follows ASK2, ASK4, FSK2, FSK4, PSK2, PSK4, QAM16 and QAM64. The thresholds of different parameters have been calculated offline for the classification the used in the algorithm in real time situation. The parameters are carefully chosen based on signal statistics. The parameters selected are

- **Absenv**

$$absEnv = \frac{1}{N}\sum_{i=1}^{N}\left|A_{cn}[i]\right|$$

- **AbsPhase**

$$absPhase = \frac{1}{C}\sum_{A_n[i]>a_t}\left|\phi_c[i]\right|$$

$$\phi_c[i] = \phi[i] - \frac{1}{N}\sum_{j=1}^{N}\phi[j]$$

- **rEnv**

$$rEnv = \frac{1}{N}\sum_{i=1}^{N}\left|A[i] - m_a\right| \Big/ m_a$$

- **absEnv2**

$$rEnv2 = \frac{1}{N}\sum_{i=1}^{N}\left|B_{cn}[i] - m_b\right|$$

$$B_{cn}[i] = \left|A_{cn}[i]\right|$$

$$m_b = \frac{1}{N}\sum_{i=1}^{N}B_{cn}[i]$$

- **absFreq**

$$absFreq = \frac{1}{C}\sum_{A_n[i]>a_t}\left|\frac{f[i] - f_a}{Fsym}\right|$$

$$f_a = \frac{1}{C}\sum_{A_n[i]>a_t}f[i]$$

- **absFreq2**

$$absFreq2 = \frac{1}{C}\sum_{A_n[i]>a_t}\left|f_2[i]-\frac{1}{C}\sum_{A_n[j]>a_t}f_2[j]\right|$$

$$f_2[i]=\left|\frac{f[i]-f_a}{Fsym}\right|$$

- **absPhase2**

$$absPhase2 = \frac{1}{C}\sum_{A_n[i]>a_t}\left|\phi_2[i]-\frac{1}{C}\sum_{A_n[j]>a_t}\phi_2[j]\right|$$

$$\phi_2[i]=\left|\phi_c[i]\right|$$

The method of classification is based on the threshold value which is calculated offline for various modulation techniques. Based on the flow chart (Refer fig.7) the type of modulation transmitted to the receiver is received.

HARDWARE USED FOR IMPLEMENTATION

FL2440 is a development board released by Witech Embedded for the Samsung S3C2440; it is split into two parts: 6-layer core board and a 2-layer application board, such structure not only makes the FL2440 more flexible but also more convenience for maintenance. The layout and wiring on the FL2440 are professionally designed, to make the FL2440 development board more stable and reliable performance. Together with the FL2440 we provide BSPs (Board Support Packages) for Embedded Linux and Windows CE including basic drivers for all the components on the board and shorten the development cycle (ref fig 1).

Software Blocks on FL2440

In this work, the implementation of various signal processing blocks is done using GNU radio.GNU radio is a free and open source software development toolkit that provides signal processing blocks to implement software radios. It can be used with readily available low cost external RF hardware to create software-defined radios or without hardware in a simulation like environment. It is widely used in hobbyist, academic and commercial environment to support both wireless communications research and real world radio systems

GNU radio applications are primarily written using the python programming language, while the supplied performance critical signal processing path is implemented in C++ using processor floating point extensions, where available. Thus, the developer is able to implement real time, high through put radio systems in a simple to use, rapid application development environment.GNU Radio provides a library of signal processing blocks and the glue to tie all together. The programmer builds a radio by creating a graph, where the vertices are signal processing blocks and the edges represent the data flow between them. The signal processing blocks are implemented in C++.Conceptually, blocks process infinite streams of data flowing from their input ports to their output ports. Blocks attributes include the number of input and output ports they have as well as the type of data that flows through each.

The most frequently used types are short, float and complex. Some blocks have only output ports or input port. These serve as data sources and sinks in the graph. There are sources that read from a file or ADC and sinks that write to a file, digital to analog converter (DAC) or graphical display. About 100 blocks come with GNU Radio. Writing new blocks is not difficult and can be easily implemented. Thus, GNU Radio can be extended.

Figure 1: S3C2440 Hardware Implementation

Design of Transmitter

The User selects one of the modulations using the "modulation selection switch" (Refer figure 6). Based on the modulation selected, the appropriate software block is activated. The data is modulated using the selected software block. The carrier is generated using the carrier generation software block. The noise variance is controllable and is generated using the noise generation software block. The modulated wave is transmitted converted to analog signal using on board DAC and the signal is transmitted using antenna.

Design of Receiver

The modulated signal is sampled through analog to digital convertor at a high sampling rate. The digitized signal is then noise filtered by noise filtering software block. The modulation scheme is detected by applying algorithms on the sampled data. Based on the detected modulation scheme, appropriate demodulation software block is activated and data is demodulated (Refer figure 7).

Blocks Used in the Present Work

Table 1

gnuradio.gr	
gnuradio. digital	gr-digital package
gnuradio.blks2	
gnuradio. audio	gr-audio package
gnuradio. Trellis	
gnuradio.wavelet	gr-wavelet package
gnuradio.fft	gr-fft package
gnuradio.window	Routines for designing window functions
gnuradio.optfir	Routines for designing optimal FIR filters
gnuradio.gr_unittest	
gnuradio.qtgui	gr-qtgui package
gnuradio.wxgui	gr-wxgui package

QAM Implementation

Pseudo Code

Step 1: Make constellations.

Step 2: For Transmitter and Receiver set the common constellations. Set QAM 4, QAM 8, QAM 16, QAM 64, QAM 256

Step 3: Check whether the constellation requires the gray code or not.

Step 4: If yes, perform binary to gray code operation. If No, do not need gray code.

Step 5: After step 4, perform the identity map.

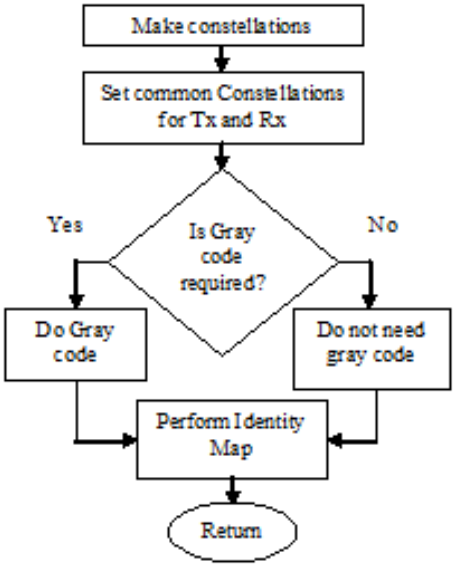

Figure 2: Flow Chart

RESULTS AND DISCUSSIONS

The results obtained by modulating the input signal (could be an image (or) video also) using S3C2440 based hardware is shown in figure 3 & 4 for QAM and ASK scheme alone. Similar results were obtained for other modulation schemes also and is not reproduced for brevity.

Case (1)

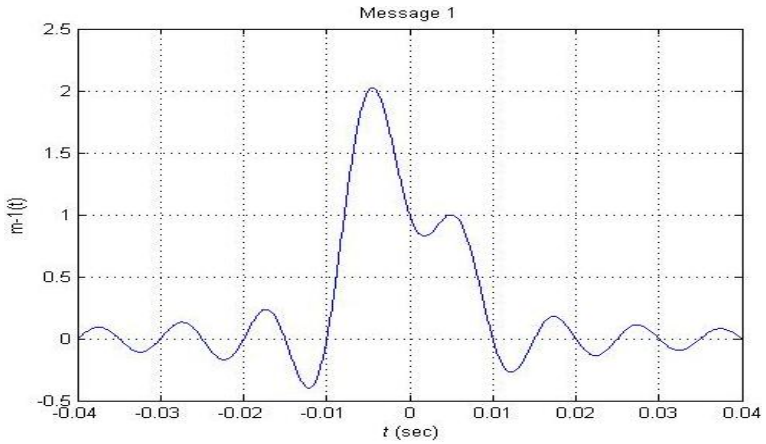

Figure 3: (a) Demodulated Signals

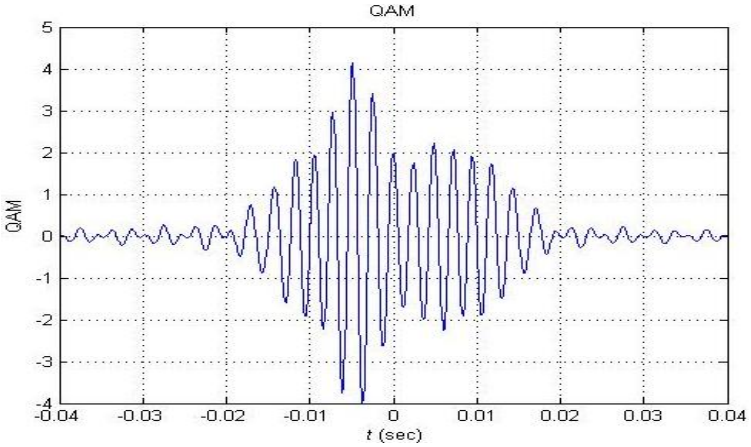

Figure 3 (b): Modulated Signal

Case (2)

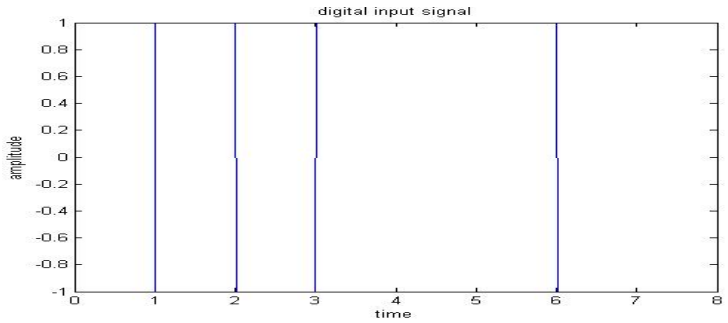

Figure 4 (a): Demodulated Signals

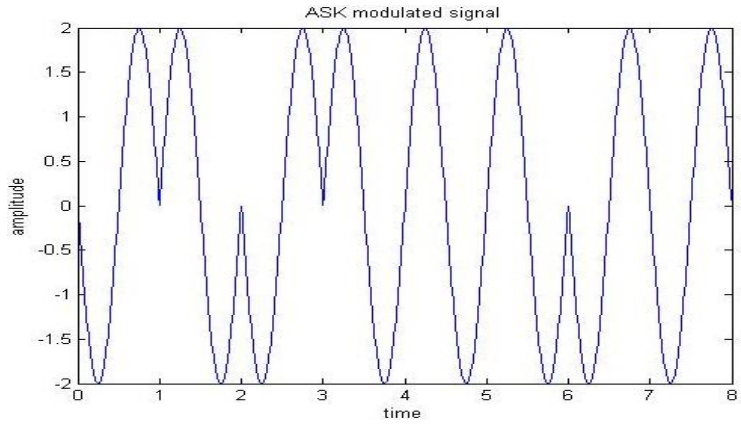

Figure 4 (b): Modulated Signal

CONCLUSIONS

In this paper, a method for automatic modulation with hardware implementation is presented. The system can inherently oppose active attacks occurring through participation in Communication / impersonate legitimate users by altering the type of modulation at required instant. Also, the security concept such as confidentiality, authenticity and availability is taken care in the work. The proposed system was tested on five different modulation schemes. The experimental results demonstrated that the proposed system provides better performance and can form a dependable core for next generation “internet of things”.

REFERENCES

1. El Moussati A, Ghoumid, K and Zaidouni J, “Hardware implementation for Turbo code-OFDM using Software defined Radio”, International Conference on Complex Systems (ICCS), 2012, pp 1-5
2. Tachwali, Y and Refai, H, “Implementation of a BPSK Transceiver on Hybrid Software Defined Radio Platforms”, 3rd International Conference on Information and Communication Technologies: From Theory to Applications, 2008,pp 1-5
3. Chilo, J. and Lindblad, T, “Hardware Implementation of 1D Wavelet Transform on an FPGA for Infrasound Signal Classification”, IEEE Transactions on Nuclear Science,vol.55,no.1, 2008, pp 9-13
4. Urriza, P, Rebeiz, E and Cabric, D, “Hardware implementation of Kuiper-based modulation level classification”, Conference Record of the Forty Fifth Asilomar Conference on Signals, Systems and Computers (ASILOMAR), 2011, pp 6-9

5. D. Dabrowski, E. Jamro and W. Cioch, "Hardware Implementation of Artificial Neural Networks for Vibroacoustic Signals Classification", ACTA PHYSICA POLONICA Acoustic and Biomedical Engineering, vol. 118, 2010, pp 41-44
6. Mustafa, H.D, Rao, C.S.Merchant, S.N and , "A novel algorithm for multiple signal classification with Optimized Coulomb Energy Neural Networks for Power line communications", IEEE International Symposium on Power Line Communications and Its Applications (ISPLC), 2010,pp.90 - 95
7. Morrison, S.A, Parks, J.S, Gugel, K.S, "A high-performance multi-purpose DSP architecture for signal processing research", Proceedings of IEEE International Conference on Acoustics, Speech, and Signal Processing, vol.2 April 2003, pp.601-604
8. Namjin Kim Kehtarnavaz, N,Yeary, M.B. and Thornton, S, "DSP-based hierarchical neural network modulation signal classification ",IEEE Transactions on Neural Networks, vol.14 , no.5 , 2003 pp.1065 – 1071.
9. Feldkamp, L.A,Dearborn and Puskorius, G.V, "A signal processing framework based on dynamic neural networks with application to problems in adaptation, filtering, and classification", Proceedings of the IEEE , vol.86, no.11, 1998,pp.2259 - 2277
10. [10] Keith E. Nolan, Linda Doyle, Philip Mackenzie and Donal O'Mahony, "Modulation Scheme Classification for 4G Software Radio Wireless Networks", Networks and Telecommunications Research Group, 2009

AUTHOR'S DETAILS

R. Kannan was born in (Arani, July 3rd, 1977). His educational background is B.E., in EEE, from Arunai Engineering College, Tiruvannamalai, Tamilnadu, India 1995 and M.E., in Applied Electronics, from Dr. M.G.R Engineering College, Chennai, Tamilnadu, India (affiliated to Madras University) in 2000. He is presently working as Asst. Professor in Annamalaiyar College of Engineering, Arani. He has got four publications and has been carrying out research in the area of software defined radio actively.

Dr. S. Ravi received DEEE, A.M.I.E (ECE), and M.E (CS) degree in the year 1989, 1991 and 1994 respectively and Doctorate degree from Anna University, Chennai in the year 2004. He is having 18 years of teaching experience. His areas of interests are VLSI, Embedded Systems, Image Processing and Simulation and Modeling. He has published more than 40 papers in International National Conferences and 30 in Journals. He is a member of IEEE and ISTE and Life member of IETE and IETUK.

APPENDICES

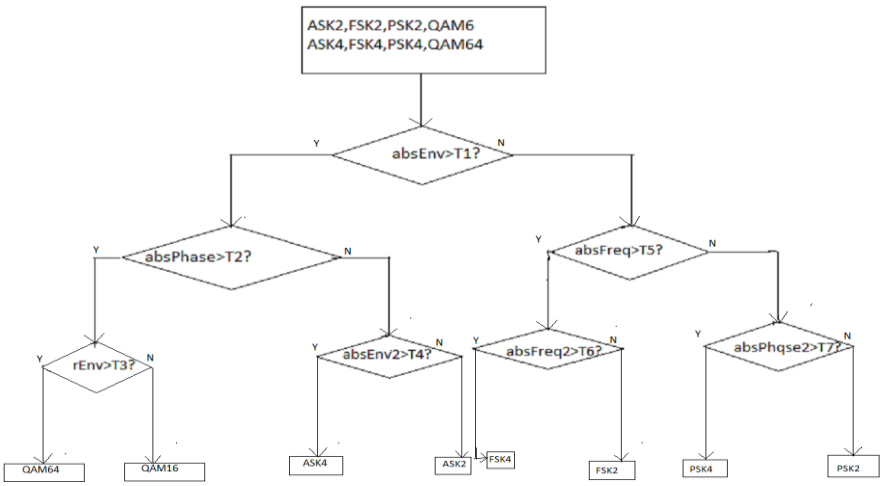

Figure 5: Flow Chart

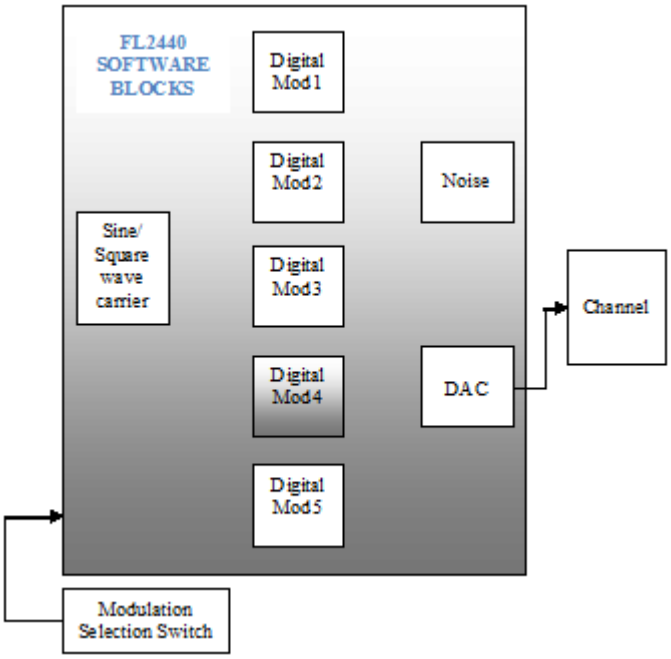

Figure 6: Block Diagram of Transmitter

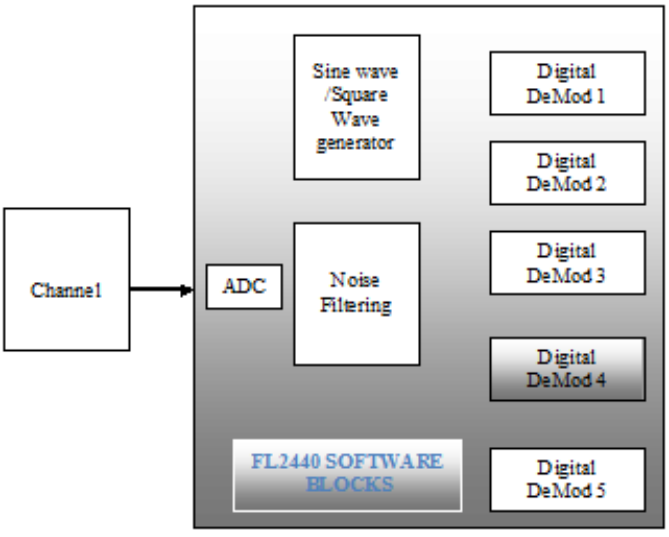

Figure 7: Block Diagram of Receiver